# Generalized Hypercube and Hyperbus Structures for a Computer Network

LAXMI N. BHUYAN, MEMBER, IEEE, AND DHARMA P. AGRAWAL, SENIOR MEMBER, IEEE

Abstract — A general class of hypercube structures is presented in this paper for interconnecting a network of microcomputers in parallel and distributed environments. The interconnection is based on a mixed radix number system and the technique results in a variety of hypercube structures for a given number of processors N, depending on the desired diameter of the network. A cost optimal realization is obtained through a process of discrete optimization. The performance of such a structure is compared to that of other existing hypercube structures such as Boolean *n*-cube and nearest neighbor mesh computers.

The same mathematical framework is used in defining a corresponding bus oriented structure which requires only two I/O ports per processor. These two types of structures are extremely suitable for local area computer networks.

Index Terms — Distributed computers, hyperbus structures, hypercube structures, local area networks, multistage interconnection networks, parallel computers, topological optimization.

## I. INTRODUCTION

SEVERAL structures have been proposed in the literature  $\mathbf{V}$  for interconnecting a large network of computers in parallel and distributed environments [2]-[12]. In this paper, we present a generalized hypercube structure and reveal some interesting properties of hypercubes. An interconnection structure in general should have a low number of links per node (degree of a node), a small internode distance (diameter), and a large number of alternate paths between a pair of nodes for fault tolerance. The distance between any two nodes is defined as the number of links traversed by a message, initiated from one node and sent to another via intermediate nodes. In a network of N nodes, the diameter is defined as  $D = \max\{d_{ii} \mid 1 \le i, j \le N\}$ , where  $d_{ii} =$ distance between nodes i and j along the shortest path. Designing a network with a low message traffic density and good modularity is also desirable.

The Boolean *n*-cube computer [7] is an interconnection of  $N = 2^n$  processors which may be thought of as placed at the corners of an *n*-dimensional cube with each edge of the cube having two processors. The degree of a node and the diameter of this type of structure are equal to  $n = \log_2 N$ . A loop structure with additional links is imbedded in this structure,

Manuscript received March 24, 1983; revised October 12, 1983. A preliminary version of this paper was presented at the 9th Annual International Symposium on Computer Architecture, April 1982.

L. N. Bhuyan is with the Department of Electrical and Computer Engineering, University of Southwestern Louisiana, Lafayette, LA 70504.

D. P. Agrawal is with the Computer Systems Laboratory, Department of Electrical and Computer Engineering, North Carolina State University, P.O. Box 7911, Raleigh, NC 27650.



Fig. 1. A Boolean *n*-cube computer with N = 8.

and for N = 8, this is illustrated in Fig. 1. When the total number of nodes N equals  $W^D$ , W and D both Being integers, the nodes can be arranged as a D-dimensional hypercube with W nodes in each dimension. If a node is connected to its two nearest neighbors in each dimension, a nearest neighbor mesh hypercube is obtained. The degree of a node in such a structure is 2D and the diameter is WD/2 for W > 2 [8]. There is also a loop structure associated with a nearest neighbor mesh as shown in Fig. 2 for a two-dimensional mesh with 9 nodes. We can also deduce that a bidirectional single loop structure [3] is equivalent to a nearest neighbor connection with dimension D = 1. This structure has a minimum number of links and a diameter of N/2. Any two nonadjacent faulty nodes will disconnect the loop. With the addition of an extra link to the loop structure the diameter is reduced to  $0(\sqrt{N})$  [4]. On the other hand, a completely connected structure has (N - 1) links per node with a distance of one between any two nodes. Any two nodes remain connected



Fig. 2. A nearest neighbor mesh with  $N = 3^2$ .

even if all other nodes fail. However, both the high cost of a large number of links and the multiport requirement of O(N) limit the size of the network.

In a multicomputer environment, the average internode distance, message traffic density, and fault tolerance are very much dependent on the diameter and degree of a node. There is a tradeoff between the degree of a node and the diameter. A structure with a low degree of a node has a large diameter and a structure that has a low diameter usually possesses a large degree of a node. A single loop structure and a completely connected structure as described above represent the two extremes. The (diameter \* degree of a node) is therefore a good criterion to measure the performance of a structure. The hypercube structures seem to offer a reasonable characteristic. One commonly noted disadvantage of the Boolean *n*-cube computer is that the number of I/O ports is  $\log_2 N$ . However, keeping in mind the simple routing, the low diameter, and the large  $(\log_2 N)$  number of disjoint paths, this topology seems extremely suitable for a local computer network. Moreover, with current advances in technology, the number of I/O ports per processor up to 1000 has become quite feasible [13]. Recently, a few structures have been proposed with better graph theoretic properties [9]-[12]. Their fault tolerance is basically limited by the fixed number of I/O ports per node. What we present here is a complete generalization of the hypercube and some interesting analyses of hypercube structures, where good fault tolerance is guaranteed. The present study should therefore be viewed in that context.

This paper presents two new hypercube structures, called

generalized hypercube (GHC) and generalized hyperbus (GHB) structures. They possess the following characteristics:

1) The interconnection supports any number of nodes N. This is in contrast with the existing hypercube structures, where  $N = W^D$  for some integer values of W and D.

2) The design is based on the allowable diameter of the network. If the diameter can be increased, a structure with a lower degree of a node can be obtained.

3) These structures are highly fault tolerant, they possess a small average message distance and a low traffic density.

4) The structures presented here are very general in nature. Single loop, Boolean n-cube, nearest neighbor mesh hypercube and fully connected systems can be considered as a part of this generalized structure.

5) The GHB structures have only two links per node, and hence require only two I/O ports per processor.

The paper is organized as follows. Section II describes a useful mixed radix number system used in [14], [15], the topology, the properties, and the routing and broadcasting algorithms of the GHC structures. Section III analyzes the GHC structures with respect to a cost parameter defined by (degree of a node) \* (diameter). The section also outlines the procedure for obtaining an optimal GHC (OGHC) structure. Section IV considers the parameters like average distance, cost, traffic density, and fault tolerance, etc. to compare the performance of an OGHC to other hypercube structures. Section V obtains the equivalent m-cube multistage interconnection networks (MIN's) of the GHC structures. Section VI presents the GHB structures and derives the expressions for internode distances.

#### II. THE GENERALIZED HYPERCUBE (GHC) STRUCTURE

#### A. A Mixed Radix Number System

Let N be the total number of processors and be represented as a product of  $m_i$ 's,  $m_i > 1$  for  $1 \le i \le r$ .

$$N = m_r * m_{r-1} * \cdots * m_1.$$

Then, each processor X between 0 to N - 1 can be expressed as an r-tuple  $(x_r x_{r-1} \cdots x_1)$  for  $0 \le x_i \le (m_i - 1)$ . Associated with each  $x_i$  is a weight  $w_i$ , such that  $\sum_{i=1}^r x_i w_i = X$  and  $w_i = \prod_{j=1}^{i-1} m_j = m_{i-1} * m_{i-2} * \cdots * m_1$  for all  $1 \le i \le r$ . Hence,  $w_1 = 1$  always.

Example 1:

Let 
$$N = 24 = 4 * 3 * 2$$
.  
 $m_1 = 2$ ,  $m_2 = 3$ ,  $m_3 = 4$ .  
 $w_1 = 1$ ,  $w_2 = 2$ ,  $w_3 = 6$ .

Then,  $X = (x_3x_2x_1)$ ,  $0 \le x_1 \le 1$ ,  $0 \le x_2 \le 2$ ,  $0 \le x_3 \le 3$ for any X in the range 0-23.  $0_{10} = (000)$ ,  $23_{10} = (321)$  in this mixed radix system.

# B. Description of the GHC Structure

Each processor  $X = (x_r x_{r-1} \cdots x_{i+1} x_i x_{i-1} \cdots x_1)$  will be connected to processors  $(x_r x_{r-1} \cdots x_{i+1} x_i' x_{i-1} \cdots x_1)$  for all  $1 \le i \le r$ , where  $x_i'$  takes all integer values between 0 to  $(m_i - 1)$  except  $x_i$  itself. This type of interconnection will be called the generalized hypercube (GHC) throughout this paper. In general, the total number of links (L) is greater than the total number of processors (N) in this GHC topology.

*Example 2:* For N = 24, any processor can be expressed in the mixed radix system between (000) and (321). Processor (000) is connected to processors (001), (010), (020), (100), (200), and (300). Processor (001) is connected to processors (000), (011), (021), (101), (201), and (301) and so on as shown in Fig. 3. For the sake of clarity, connection is not completed in the figure for the nodes shown by dotted lines. Imbedded in this structure is a loop structure arranged as  $(000) \rightarrow (001) \rightarrow (011) \rightarrow (021) \rightarrow (121) \rightarrow (221) \rightarrow$  $(321) \rightarrow (311) \rightarrow (301) \rightarrow (300) \rightarrow (310) \rightarrow (320) \rightarrow$  $(220) \rightarrow (120) \rightarrow (020) \rightarrow (010) \rightarrow (110) \rightarrow (210) \rightarrow$  $(200) \rightarrow (201) \rightarrow (211) \rightarrow (111) \rightarrow (101) \rightarrow (100) \rightarrow$ (000) with 4 extra links per node.

The GHC structure consists of *r*-dimensions with  $m_i$  number of nodes in the *i*th dimension. A node in a particular axis is connected to all other nodes in the same axis. Accordingly, we make the following observations.

1) From any particular node  $X = (x_r x_{r-1} \cdots x_{i+1} x_i x_{i-1} \cdots x_1)$ , there are  $(m_i - 1)$  number of links in the *i*th direction. Hence, for all  $i, 1 \le i \le r$ , the total number of links per node or the degree of a node  $\ell = \sum_{i=1}^{r} (m_i - 1)$ .

2) Each link is connected to two processors. Hence, the total number of links in GHC structure  $L = N/2 \cdot \sum_{i=1}^{r} (m_i - 1)$ .

3)  $d_{xy}$  = distance between any two nodes x and y in terms of number of hops = Hamming distance between the nodes. Hamming distance between two nodes differing in their addresses in the *i*th coordinate only is unity and the total Hamming distance is the sum of the number of coordinates in which the addresses differ.

4) The addresses can differ at maximum in all the r-coordinates. Thus, the diameter of the structure = r.

## C. Routing Procedure

A message is formatted at the source node with source address, destination address and a few tag bits. The source and destination addresses are specified in the binary equivalent of the mixed radix numbers. The *i*th digit of the address can take a maximum value of  $(m_i - 1)$ , and hence can be expressed in  $\lceil \log_2 m_i \rceil$  binary bits, where  $\lceil x \rceil$  is the smallest integer greater than or equal to x. As a result, any processor  $0 \le X \le N - 1$  can be specified completely in  $\sum_{i=1}^{r} \lceil \log_2 m_i \rceil$  binary bits. At each node, the destination address is compared to its own address, contained in a register. If the addresses match, the node accepts the message. If they do not, a digit by digit comparison takes place and the node transmits the message along the direction of the first differing digit. The process continues until the destination is reached. However, at each node the message goes through a certain delay, waiting for the particular link to be free.

Based on the above routing procedure, we can deduce the following.

1) If two nodes differ in their address by d coordinates (dimensions), then d is the shortest distance between these two nodes. A message can start from the source node along



any one of these d coordinates and then follow the above routing procedure to reach the destination node. These paths, illustrated in Fig. 4(a), are disjoint and cover a distance deach. This observation is similar to the characteristics of a Boolean *n*-cube computer [16].

2) From any node  $(x_r x_{r-1} \cdots x_i \cdots x_2 x_1)$ , the message can go to an intermediate neighboring node and travel to the corresponding neighboring node of the destination  $(y_r y_{r-1} \cdots y_i \cdots y_2 y_1)$ . In the previous case, a message could start along a particular node in the *i*th coordinate only if the source and destination addresses differed in their *i*th coordinate. Note in Fig. 4(b), that a message can start along any of the nodes in the *i*th coordinate for  $1 \le i \le r$  without depending on whether or not the source and destination addresses mismatch in their *i*th coordinate. Then the intermediate nodes encountered on a single path have their *i*th coordinate fixed at a particular digit. The paths are therefore disjoint. A suitable reference to the path generation process is [10]. Hence, there are  $\ell$  alternate paths between any two nodes of the GHC structure where " $\ell$ " is the degree of a node.

3) For any number of faults less than " $\ell$ " in the system, the worst case distance between two connected nodes is r + 1. This is also clear from Fig. 4(b).

Alternate Routing Procedures: As mentioned above, there are d disjoint paths of equal length d between any two nodes separated by Hamming distance d. If the channels in one path are busy or faulty, a message can be routed in a different path with the same distance d. This is possible if the status of every link is updated at each node. In that case, the source node can route the message along an alternate path thus saving the delay in transmission. This process requires additional hardware and software and the path computation may be time consuming. If the link is busy another simple method is to route the message along the next digit of the first differing digit. For example, with N = 24, while routing from (001) to (221), instead of routing through (021) first, the message can be routed to (201) and then to (221), if the previous channel is busy.

# D. Broadcasting

Any processor can send a message to all other processors in just r steps by using the following algorithms.

The structure is an r-dimensional hypercube with  $(m_i - 1)$ 



Fig. 4. (a) "d" disjoint paths of length "d" each between nodes at Hamming distance "d." (b) "ℓ" alternate paths between any source and destination.

numbers of links in the *i*th dimension. Each link in the machine is numbered, with the links in the *i*th dimension being numbered "*i*" for all  $1 \le i \le r$ . Let us assume node A  $(00 \cdots 0)$  wishes to broadcast a message. To do so, it sends messages with a weight "*i*" in the links along the *i*th dimension. In the second step, all the receiving nodes reduce the weight by one and transmit the messages along all those dimensions whose numbers do not exceed the reduced weight. The process continues for *r* steps until all the nodes have received the message. It may be noted that *r* is the lower bound for the minimum number of steps required for broadcasting in a graph with a diameter of *r*.

*Example 3:* The structure for N = 24 is shown in Fig. 3. In the first step, nodes (001) will receive the message with a weight "1," nodes (010) and (020) will receive the message with weight "2," and nodes (100), (200), (300) will receive the message with weight "3." In the next step, all these nodes will reduce their weights by one and transmit the messages as shown below.

 $(001) \rightarrow$  no transmission (010) and (020)  $\rightarrow$  (011) and (021) respectively with weight "1" (100), (200) and (300)  $\rightarrow$  (101), (201) and (301) respectively with weight "1," and (110), (120), (210), (220), (310) and (320) with weight "2."

In the third and final step,

$$(110) \rightarrow (111), (120) \rightarrow (121), (210) \rightarrow (211),$$
  
 $(220) \rightarrow (221), (310) \rightarrow (311), (320) \rightarrow (321)$  with weight "1."

The complete broadcasting is achieved in three steps, as shown in Fig. 5.

# III. ANALYSIS OF GHC STRUCTURES

# A. Structure Optimization

When an interconnection of N processors is desired with the constraint that the maximum distance between any two nodes along the shortest path or the diameter does not exceed r, N has to be expressed as a product of r quantities as  $N = m_r * m_{r-1} * \cdots * m_1$ . The number of links per node =  $\sum_{i=1}^{r} (m_i - 1)$ . In fact, there are several ways to factor N into r components. For example, 16 can be factored as 8 \* 2or 4 \* 4. An optimized structure with diameter r is obtained when the total number of links in the structure is at the minimum.

Lemma 1: When  $\sqrt[n]{N}$  is an integer, a cost optimal GHC with diameter "r" is obtained if  $m_i = \sqrt[n]{N}$  for all  $1 \le i \le r$ .

*Proof:* Since the number of links per node " $\ell$ " is the same for all the nodes, a minimization of " $\ell$ " with respect to  $m_i$ 's gives the desired result

$$m_1 = \frac{N}{m_r m_{r-1} \cdots m_2}$$
$$\ell = \sum_{i=2}^r (m_i - 1) + \left(\frac{N}{m_r m_{r-1} \cdots m_2} - 1\right)$$
$$\frac{\partial \ell}{\partial m_r} = \frac{\partial \ell}{\partial m_{r-1}} = \frac{\partial \ell}{\partial m_2} = 0.$$

This results in  $m_r = m_{r-1} = \cdots = m_2 = m_1 = \sqrt[4]{N}$ . Q.E.D. Since  $\sqrt[4]{N}$  may not be an integer, all  $m_i$ 's should lie as close to  $\sqrt[4]{N}$  as possible. When  $N = m^r$ , the mathematics involved is simply a higher radix system, each  $x_i$  lying between 0 and (m - 1) for all  $1 \le i \le r$ .

There is another aspect of the GHC structures. The number of links per node is different for different values of diameter



Fig. 5. (a) Broadcasting at the first step, (b) broadcasting at the second step, (c) broadcasting at the third step.

r. Again, for example, 16 can be expressed as 4 \* 4, 4 \* 2 \* 2, 2 \* 2 \* 2 \* 2 with diameters 2, 3, and 4, respectively. As mentioned earlier, a structure with a lower degree of a node usually has a higher diameter. If a cost factor  $\xi$  is defined as the product of the diameter and the links per node, a discrete optimization of  $r \sum_{i=1}^{r} (m_i - 1)$  with respect to r and subject to the constraint that  $\prod_{i=1}^{r} m_i = N$  and integer values of  $m_i$ 's, yields an optimized structure. As an example, the optimal values of r for processors equal to  $2^{D}$  and  $3^{D}$ , are plotted in Fig. 6. Because of the discrete optimization involved, it was not possible to derive a closed form solution for  $r_{opt}$ .

Conjecture 1: For N, a power of two, an absolute cost optimal GHC (OGHC) is obtained when  $r = \lfloor \log_4 N \rfloor$ , where |x| is the largest integer smaller than or equal to x.

This deduction follows from Fig. 6. Up to  $N = 2^3$ ,  $r_{opt} = 1$  indicates a fully connected system. For  $N = 2^4$ ,  $r_{opt} = 2$ 



results in a two-dimensional GHC with 4 nodes in each dimension. For  $N = 2^5$ , there are 4 nodes in one dimension and 8 nodes in the other. For  $N = 2^6$ ,  $r_{opt} = 3$  and so on. Also, for N and m powers of two a GHC with m nodes in each dimension has a cost of  $(m - 1) \log_m^2 N$  which has a local minimum at m = 4.

For N, a power of four, the degree of a node of an OGHC is  $3 \log_4 N = 1.5 \log_2 N$ . The diameter is  $\log_4 N = 0.5 \log_2 N$ . Hence, the cost = 0.75  $(\log_2^2 N)$ . The cost of other structures [9]-[12] are proportional to  $(\log_2 N)$  instead of  $(\log_2^2 N)$ . However, they do not possess as good a fault tolerance as the GHC structures do. For N, a power of 5, the cost is  $0.742 \log_2^2 N$  when m = 5. However, only values of N which are powers of two are considered in conjecture 1 for later use in Section IV.

# B. Internode Distance and Queueing Delay

Distance between any processor  $X = (x_r x_{r-1} \cdots x_{i+1} x_i x_{i-1} \cdots x_2 x_1)$  and  $X' = (x_r x_{r-1} \cdots x_{i+1} x_i', x_{i-1} \cdots x_2 x_1)$ ,  $x_i' \in \{0, 1, 2, \dots, m_i - 1\}$  and  $x_i' \neq x_i$ , is unity. In general, the distance between any two processors is equal to the Hamming distance between them; that is, in how many coordinates their addresses differ. The average internode distance plays a key role in determining the queueing delay in a computer network. For calculating the number of nodes at different distances, the node  $(00 \cdots 0)$  can be assumed to be the source node without any loss in generality. There are  $(m_i - 1)$  number of nodes which differ from the source node only in the *i*th dimension. Hence,  $N_1$  = total number of nodes differing by distance 1

$$=\sum_{i=1}^r (m_i-1).$$

The nodes which have distance 2 from the source node must differ in their addresses by two coordinates *i* and *j*. In these two dimensions,  $(m_i - 1)(m_j - 1)$  different combinations can occur. Again, these two dimensions are selected out of *r* such dimensions existing in the address space. Hence, the total number of nodes differing by the shortest distance 2,

$$N_2 = \sum (m_i - 1) (m_j - 1)$$
  
i, j  $\varepsilon \{1, 2, \dots, r\}$  and  $i \neq j$ .

There are  $\binom{r}{2}$  terms to be added in this summation. The same ideas can be extended to calculate the number of nodes differing by a Hamming distance d,

$$N_d = \sum (m_i - 1) (m_j - 1) (m_k - 1) \cdots d \text{ such terms}$$
$$i, j, k \cdots \varepsilon \{1, 2, \cdots, r\}$$
$$i \neq i \neq k \neq \cdots$$

and the summation includes  $\binom{r}{d}$  such items.

A Boolean *n*-cube structure can be considered as a special case of GHC structures, where  $m_i = 2$  for  $1 \le i \le r$ . As a result,  $N = 2^r$  and  $r = \log_2 N = n$ .

$$\prod (m_i - 1) = 1 \quad \text{and} \quad N_d = \binom{n}{d} = \frac{n!}{d!(n-d)!}.$$

Once the number of nodes at a distance d is known, the average message distance is  $\overline{d} = (\sum_{d=1}^{r} dN_d)/(N-1)$ .

To get an idea how the average message distance varies, let us consider the case when  $N = m^r$ . Also, as mentioned earlier,  $m_i$ 's should be as close as possible to  $\sqrt[r]{N}$  for an optimized structure with diameter r, and hence this should give approximate results for any N that can be factored into r-components.

When all  $m_i$ 's are equal to m, the number of nodes at a distance d,  $N_d = {\binom{r}{d}(m-1)^d}$ , and

$$\overline{d} = \left[\sum_{d=1}^{r} d\binom{r}{d} (m-1)^{d}\right] / (N-1)$$

$$= (m-1) \left[\sum_{d=0}^{r} \binom{r}{d} \frac{\partial (m-1)^{d}}{\partial (m-1)}\right] / (N-1)$$

$$= (m-1) \frac{\partial}{\partial (m-1)} \left[\sum_{d=0}^{r} \binom{r}{d} (m-1)^{d}\right] / (N-1)$$

$$= \left[(m-1) \frac{\partial}{\partial (m-1)} (m-1+1)^{r}\right] / (N-1)$$

$$= r \cdot (m-1) \cdot m^{r-1} / (N-1), \qquad m = \sqrt[r]{N}.$$

Fig. 7 shows the variation of average message distance  $(\overline{d})$  with respect to r for a few values of m. When m = 2, it is simply a Boolean *n*-cube structure. For an OGHC,  $\overline{d} \approx 0.375 \log_2 N$ .

The average message traffic density in a link of GHC structures is defined as

$$\rho = \frac{\text{Average message distance * number of nodes}}{\text{total number of links}}$$
$$= \frac{\overline{dN}}{\frac{N}{2} \sum_{i=1}^{r} (m_i - 1)} = \frac{2\overline{d}}{\sum_{i=1}^{r} (m_i - 1)}.$$

For  $N = m^r$ ,  $\rho = \frac{2\overline{d}}{r(m-1)} = 0.5$  for an OGHC structure.

The GHC structures can be modeled as a communication net with the *i*th channel represented as an M/M/1 system with Poisson arrivals at a rate  $\lambda_i$  and exponential service time of mean  $1/\mu c_i$  [17].  $\mu$  = average service rate and  $c_i$  =



Fig. 7. Average message distance in GHC-structure with  $N = m^{r}$ .

capacity of the *i*th channel. Additionally, we assume the following.

1) Each node is equally likely to send a message to every other node in a fixed time period.

2) The routing is done as per the fixed routing algorithm described in Section II.

3) The load is evenly distributed, i.e.,  $\lambda_i$  is the same for all *i*.

4) The capacity of each link in the network has been optimally assigned [17].

5) The cost per capacity per link is unity.

Under the above conditions, the delay of GHC structures is given by [17]

$$T = \frac{\overline{d} \left( \sum_{i=1}^{M} \sqrt{\frac{\lambda_i}{\lambda}} \right)^2}{\mu C (1 - \overline{d} \gamma)}$$

where

M = total number of directed links,

 $\lambda = \sum_{i=1}^{M} \lambda_i = M \lambda_i$  because of assumption 3),

 $\gamma$  = the utilization factor, and

 $C = \sum_{i=1}^{M} c_i$  = total capacity of the structure.

With N nodes and  $\ell$  bidirectional links per node,

$$M=\left(\frac{N}{2}\right)\cdot 2\ell.$$

Hence,

$$T = \frac{\overline{d}\left(\frac{N}{2}\right) \cdot 2\ell}{\mu C(1 - \overline{d}\gamma)}$$

With constants  $\mu$ , C, and N, the above delay can be normalized as

$$T' = \frac{\overline{d}2\ell}{(1-\overline{d}\gamma)}.$$

The delay increases exponentially with increased utilization and saturates at a particular load, given by  $\gamma_{sat} = 1/\overline{d}$ . In a fully connected system,  $\gamma_{sat} = 1$  since  $\overline{d} = 1$ , and hence the computer network performs very well under heavy load con-



Fig. 8. Normalized queueing delay in GHC-structures with N = 16.

ditions. In general, the performance of the GHC structures will lie between a loop structure and a fully connected net. The average delay in different GHC structures for N = 16 is plotted in Fig. 8. As expected, the optimized structure with N = 4 \* 4, performs well both in light load and heavy load conditions. Table I presents a summary of some relevant information for different GHC structures with N = 16 and 24.

## IV. PERFORMANCE OF GHC STRUCTURES

In this section, the performance of the GHC structures will be compared to that of other hypercube structures. The number of nodes N will be assumed to be a power of two and the GHC considered here is the OGHC as obtained in Section III. The loop structure is a nearest neighbor mesh in one dimension, whereas a completely connected structure is a one-dimensional GHC. The Boolean *n*-cube computer, although it is a part of the GH and the nearest neighbor mesh, is a well known topology and will therefore be considered separately. The nearest neighbor mesh considered here is an optimal structure as described below.

Nearest Neighbor Mesh Hypercube Structures: If N can be expressed as a product of r-terms, a generalized nearest neighbor mesh hypercube is obtained when a node  $(x_r x_{r-1} \cdots x_{i+1} x_i x_{i-1} \cdots x_2 x_1)$  is connected to  $[x_r x_{r-1} \cdots x_{i+1} (x_i + 1) \mod m_i x_{i-1} \cdots x_2 x_1]$  and  $[x_r x_{r-1} \cdots x_{i+1} (x_i - 1) \mod m_i x_{i-1} \cdots x_2 x_1]$  for all  $1 \le i \le r$ . Such a structure for N = 4 \* 3 \* 2 is shown in Fig. 9. The degree of a node is 2r when all the factors are greater than two. The diameter of such a structure is  $\sum_{i=1}^{r} \lfloor m_i/2 \rfloor$ . For a fixed value of N, there can be several ways to factor N into r components. The degree of a node being fixed at 2r, an optimal structure is obtained when  $\sum_{i=1}^{r} \lfloor m_i/2 \rfloor$  is minimum. For high values of  $m_i$ , the floor function can be neglected. The following lemma results.

Lemma 2: An optimal nearest neighbor mesh with some fixed r dimensions is obtained when  $m_i \cong \sqrt[r]{N}$ .

Again, for a fixed value of N, there can be several ways to design a nearest neighbor mesh. A discrete optimization of the product of the degree of a node and the diameter, for various values of r, will give rise to an optimal design. The

TABLE I CHARACTERISTICS OF GHC STRUCTURES

N	Factors	Diameter r	Links per node ℓ	Cost Factor ξ	Average Message Distance $\overline{d}$	$\gamma_{ m sat}$
	2 * 2 * 2 * 2	4	4	16	2.13	0.47
16	4 * 2 * 2	3	5	15	1.87	0.535
	4 * 4	2	6	12	1.6	0.625
	16 (fully connected)	1	15	15	1	1
24	3 * 2 * 2 * 2	4	5	20	2.26	0.442
	4 * 3 * 2	3	6	18	2.0	0.5
	6 * 4	2	8	16	1.65	0.606
	24 (fully connected)	1	23	23	1	1



Fig. 9. A generalized nearest neighbor mesh hypercube with N = 4 \* 3 \* 2.



Fig. 10.  $r_{opt}$  for nearest neighbor mesh hypercube with  $N = m^{D}$ .

values of  $r_{opt}$  for N, powers of 2 and 3 are plotted in Fig. 10. For N, a power of two, an optimal structure is obtained when there are 8 nodes in each dimension, as can be seen from the computation.

Conjecture 2: For N, a power of two, an optimal nearest neighbor mesh hypercube is obtained when  $r = \lceil \log_8 N \rceil$ .

Throughout this section, such an optimal structure (8-cube) will be considered for performance comparison. Average Message Distance  $(\overline{d})$ :

Loop: 
$$\overline{d} = \frac{2\left(1+2+3+\dots+\frac{N-1}{2}\right)}{N-1}$$
  
 $= \frac{1}{4}(N+1) \text{ for } N \text{ odd}$   
 $= \frac{2\left(1+2+3+\dots+\frac{N-2}{2}\right)+\frac{N}{2}}{N-1}$   
 $= \frac{1}{4}\frac{N(N-2)}{N-1} \text{ for } N \text{ even}$   
 $\cong 0.25 N \text{ for any } N.$   
Boolean *n*-cube:  $\overline{d} = \sum {n \choose d} d = \frac{n}{2} \cdot \frac{N}{N-1}$ 

B

$$\approx 0.5 \log_2 N$$
.

Nearest neighbor mesh:

With N = W', the maximum distance along each direction is W/2. The average distance along each dimension is 0.25 W as in the case of a loop. For r dimensions,  $\overline{d} \approx 0.25 \ rW$ . With an optimal design, W = 8 and  $\overline{d} = 0.25 \times \log_8 N \times$  $8 = 0.667 \log_2 N.$ 

OGHC:  $\overline{d} = 0.375 \log_2 N$ . Completely connected:  $\overline{d} = 1$ . Cost:

The cost of a structure = degree of a node \* diameter Loop: Degree of a node = 2, Diameter = 0.5N. Hence,  $\cos t = N$ . Boolean *n*-cube: Degree of a node = Diameter =  $\frac{1}{2}$  $\log_2 N$ , cost =  $\log_2^2 N$ . Nearest neighbor mesh: Degree of a node =  $2 \log_8 N =$  $0.667 \log_2 N$ Diameter =  $r \cdot (W/2) =$  $4 \log_8 N = 1.333 \log_2 N$  $Cost = 0.889 \log_2^2 N.$ OGHC: Cost =  $0.75 \log_2^2 N$ . Completely connected: Cost = N - 1. Average message traffic density: Average message traffic density  $\rho = (\overline{d} \times N)/L$ 

Loop: Number of links L = N; hence  $\rho = \overline{d} = 0.25N$ Boolean *n*-cube:  $L = 0.5N \log_2 N$ ;  $\rho =$  $\bar{d}/0.5 \log_2 N = 1$ Nearest neighbor mesh:  $L = r \cdot N = 0.334N \log_2 N$  $\rho = \overline{d} / 0.334 \log_2 N = 2.$ *OGHC*:  $\rho = 0.5$ .

Fault Tolerance: The fault tolerance of a structure is the connectivity or the number of node disjoint paths between any two nodes. The connectivity for a loop is 2; for a Boolean *n*-cube, it is  $\log_2 N$ ; for a nearest neighbor mesh it is 2r [18], i.e., 0.667  $\log_2 N$  here; for an OGHC it is 1.5  $\log_2 N$  and for a completely connected structure it is (N-1).

### V. *m*-CUBE INTERCONNECTION NETWORKS

An  $N \times N$  multistage interconnection network (MIN) [19]-[21] is capable of connecting N number of processing elements (PE's) to N number of memory modules (MM's). Various MIN's described in the literature [19] employ 2-input 2-output switching elements (SE's). Here, we illustrate the use of GHC structures in designing  $N \times N$  MIN's implemented with  $m \times m$  SE's. We limit our discussions to only values of N and m which are powers of two.

An *m*-cube multicomputer is a GHC structure with *m* number of nodes in each dimension. When N is a power of m, there are m nodes in each of  $r = \log_m N$  dimensions of the hypercube. When N is not a power of m, there will be  $r-1 = \lfloor \log_m N \rfloor$  dimensions with m nodes each and one dimension with  $N/_m r - 1$  number of nodes. All the nodes in a dimension are connected to each other by dedicated links. A completely connected multicomputer corresponds to a crossbar [22] in a circuit switched multiprocessor. When an m-cube GHC is unfolded, an m-cube MIN results. By unfolding we mean that the *i*th stage of the MIN is connected as per the *i*th dimension of the GHC structure for  $1 \le i \le r$ . An *m*-cube MIN will consist of  $\log_m N$  stages of N/mnumber of  $m \times m$  crossbar modules at each stage when N is a power of m. When N is not a power of m, there will be  $\lfloor \log_m N \rfloor$  stages of  $m \times m$  crossbar modules followed by  $N/_{m}r - 1 \times N/_{m}r - 1$  crossbar modules at the last stage. This also results by unfolding an m-cube GHC. The construction of a  $32 \times 32$  4-cube MIN is illustrated in Fig. 11. When a Boolean *n*-cube structure with m = 2 is unfolded, a generalized cube interconnection network [20] results. Some recent studies [15], [23], [24] have shown that a 4-cube MIN gives optimal performance in terms of bandwidth and cost.

#### VI. GENERALIZED HYPERBUS (GHB) STRUCTURES

In the preceding section, N specifies the number of processors in the structure. If, however, it specifies the number of buses, a different configuration results. Then, each processor is connected to two adjoining buses, running in different dimensions of the generalized hypercube. Such a structure for N = 3 \* 2 is shown in Fig. 12. These types of structures will be referred to as generalized hyperbus (GHB) structures. The number of processors P in a GHB structure will be greater than the number of buses N. The distance between two processors is specified by the number of buses a message has to travel from one processor to the other. Since GHB structures have fewer links than nodes, these structures will give rise to a high message traffic density in a bus, and hence will saturate rapidly. However, having only two I/O





Fig. 11. (a) A 4 \* 3 \* 2 GHC structure, (b) a  $32 \times 32$  4-cube network.

ports per processor, the cost is very small as compared to the GHC structures.

The GHB structure consists of N buses with  $N = m_r * m_{r-1} * \cdots * m_i * \cdots * m_2 * m_1$ . A bus in the GHB structure is denoted by an r-tuple  $(x_r x_{r-1} \cdots x_i \cdots x_2 x_1)$  for  $0 \le x_i \le m_i - 1$  for  $1 \le i \le r$ . A processor will be denoted  $(x_r x_{r-1} \cdots x_{i+1} [y_i z_i] x_{i-1} \cdots x_1)$ , i.e., with  $x_i$  replaced by a 2-tuple  $[y_i z_i]$  for  $y_i, z_i \in \{0, 1, \cdots (m_i - 1)\}$ . This means that the processor is connected to buses  $(x_r x_{r-1} \cdots x_1)$ .  $x_{i+1} y_i x_{i-1} \cdots x_1)$  and  $(x_r x_r - 1 \cdots x_{i+1} z_i x_{i-1} \cdots x_1)$ .  $y_i, z_i \in \{0, 1, \cdots, (m_i - 1)\}$  and the *i*th position can vary between 1 and r. The Hamming distance between a pair  $[y_i z_i]$ and some  $v_i$  is 0 if  $v_i$  is equal to  $y_i$  or  $z_i$  or  $[y_i w_i]$  or  $[w_i z_i]$  and equals 1, otherwise. Similarly, Hamming distance between  $x_i$ and  $v_i$  is 0 if  $x_i = v_i$  and equals 1 if  $x_i \neq v_i$ . The actual distance between any two different processors = Hamming distance between them +1.



The GHB structures have the following features: 1) Each processor has only two I/O ports.

2) The number of processors connected to a bus is

$$p=\sum_{i=1}^r (m_i-1).$$

3) Total number of processors in the system.

$$P = \frac{N}{2} \sum_{i=1}^{r} (m_i - 1).$$

4) Two processors can differ in their addresses in all the r-coordinates. Thus, the diameter of the structure = r + 1.

5) There are p bus disjoint paths between any two buses. A bus disjoint path also corresponds to a node disjoint path.

6) There are d disjoint paths of equal distance d between any two buses with a Hamming distance d.

7) A processor is disconnected if both the adjoining buses fail.

Internode Distance: Since the structure is symmetrical, let us consider  $0^{r-1}$  [01] as the source node.  $0^{r-1}$  means  $000\cdots$  up to (r-1) terms.

Nodes differing by unit distance:

1) When nodes have addresses  $\{w0\}$  and  $\{w1\}$ , where w is a set of (r-1) terms  $000\cdots [0x_i]\cdots 0$  for all

 $1 \le x_i \le (m_i - 1)$  and  $2 \le i \le r$ . The number of such nodes  $= 2 \sum_{i=2}^{r} (m_i - 1)$ 

2) When the nodes are of the form  $\{0^{r-1}[0x_1]\}$  or  $\{0^{r-1}[1x_1]\}$ ,  $x_1 \in \{2, 3, \dots, (m_1 - 1)\}$ . The number of such nodes  $= 2(m_1 - 2)$ . Hence, the total number of nodes with distance 1

$$N_1 = 2 \sum_{i=2}^{r} (m_i - 1) + 2(m_1 - 2).$$

When  $N = m^r$ ,  $N_1 = 2(r - 1)(m - 1) + 2(m - 2) = 2rm - 2r - 2$ .

Nodes differing by distance d:

When  $N = m_r * m_{r-1} * \cdots * m_1$ , it is extremely difficult to derive closed form expressions for  $N_d$ . Let us consider  $N = m^r$  with  $m_i = m$ ,  $1 \le i \le r$ . There are several possibilities as discussed below.

1) Nodes of the form  $\{w[0x_1]\}\$  and  $\{w[1x_1]\}\$ , where w is a r-1 tuple differing from  $0^{r-1}$  in (d-1) dimensions. For each  $[0x_1]$  and  $[1x_1]$  in the least significant digit (lsd), there are  $\binom{r-1}{d-1}(m-1)^{d-1}$  number of nodes and there are (m-1) such [0x] and (m-2) such [1x] in the lsd. Hence, number of nodes  $= (2m-3)\binom{d-1}{d-1}(m-1)^{d-1}$ .

2) Nodes of the form  $\{w0\}$  or  $\{w1\}$ .

(a) When w contains one  $[0x_i]$  in the *i*th dimension for  $2 \le i \le r$ . As a result of  $[0x_i]$  in the *i*th dimension, the node must differ in its address by (d - 1) places out of (r - 2) dimensions. There are (r - 1) values *i* can take and there are (m - 1) different values for  $x_i$ . Hence, the number of nodes  $= 2(r - 1)\binom{r-2}{d-1}(m - 1)^{d-1}(m - 1)$ .

(b) When w contains [yz],  $y, z \neq 0$  in the *i*th dimension. There are  $\binom{m-1}{2}$  such elements possible in one dimension and for each [yz] there are  $\binom{r-2}{d-2}(m-1)^{d-2}$ . Again, [yz] can occupy (r-1) dimensions except 1sd and the total number of nodes  $= 2(r-1)\binom{m-1}{d-2}\binom{m-1}{d-2}(m-1)^{d-2}$ .

3) Nodes of the form  $\{wx\}, x \in \{2, 3, \cdots (m-1)\}$ .

(a) When w contains [0y] in the *i*th dimension, for each x in the lsd, there can be (m - 1) such [0y] in a particular dimension. The number of nodes for each such  $[0y] = \binom{r-2}{d-2}(m-1)^{d-2}$ . There are (r-1) dimensions and (m-1) number of [0y] in each dimension; number of nodes for each  $x = (r-1)(m-1)\binom{r-2}{d-2}(m-1)^{d-2}$ . Again, there can be (m-2) such x in the lsd. Hence, the total number of nodes  $= (m-2)(r-1)(m-1)\binom{r-2}{d-2}(m-1)^{d-2}$ .

(b) When w contains [yz],  $y, z \neq 0$  in the *i*th dimension, there can be  $\binom{m-1}{2}$  such pairs in each dimension with each having  $\binom{r-2}{d-3}(m-1)^{d-3}$  nodes. For (r-1) such dimensions and (m-2) such x in the lsd, the total number of nodes  $= (m-2)(r-1)\binom{m-1}{2}\binom{r-2}{d-3}(m-1)^{d-3}$ .

4) Nodes of the form  $\{w[yz]\}, y, z \in \{2, 3, \dots (m-1)\}$ . There are  $\binom{m-2}{2}$  such pairs in the lsd. For each pair there will be  $\binom{r-1}{d-1}(m-1)^{d-2}$  nodes differing by distance d. Hence, the total number of nodes  $= \binom{m-2}{2}\binom{r-1}{d-2}(m-1)^{d-2}$ .

The total number of nodes  $N_d$  differing by a distance d in the GHB structure will be the sum of all the nodes in the above four possibilities. The maximum possible distance = r + 1. The total number of nodes in GHB struc-

ture with  $N = m^r$ 

$$P = 1/2 \cdot N \cdot r(m-1)$$

Hence, the average message distance is

$$\bar{d} = 2\left(\sum_{d=1}^{r+1} dN_d\right)/N \cdot r \cdot (m-1).$$

The average message traffic density in a bus in GHB structure is

$$\rho = \frac{\overline{d} \cdot \frac{N}{2} \cdot \sum_{i=1}^{r} (m_i - 1)}{N} = 1/2 \cdot \overline{d} \sum_{i=1}^{r} (m_i - 1)$$

and when  $N = m^r$ ,  $\rho = 1/2 \cdot \overline{d} \cdot r(m-1)$ .

## VII. CONCLUSION

Two types of hypercube structures, generalized hypercube (GHC) and generalized hyperbus (GHB) have been presented in this paper. The GHC structure has a low cost compared to other hypercube structures. Because of its high connectivity, the fault tolerance is quite good. It also has a low average message distance and a low traffic density in the links. These factors increase approximately as  $\log N$ . In general, the performance of GHC structure lies between that of a loop and a completely connected structure. In a GHC design it is impossible to have degree of a node less than  $\log_2 N$ . The GHB structures are obtained when a node in the GHC is replaced by a bus and a link in GHC is replaced by a node. Hence, traffic density on a bus in a GHB structure may be quite high. However, the number of I/O ports per processor is fixed at two. A generalized spanning bus hypercube [8] can similarly be obtained when each node is connected to 'r' buses, each spanning a different dimension in the address space and  $m_i$ number of nodes sharing a bus in the *i*th direction. The nodes will have identical addresses except in their *i*th coordinate.

The study provides clean design methodologies for a computer network based on the desired diameter. It also reveals many interesting properties of the hypercubes.

#### ACKNOWLEDGMENT

The authors are thankful to R. Finkel and W. Leland of the University of Wisconsin, Madison for their constructive criticisms and helpful comments.

#### References

- L. N. Bhuyan and D. P. Agrawal, "A general class of processor interconnection strategies," in *Proc. 9th Annu. Int. Symp. on Comput. Arch.*, Austin, TX, Apr. 1982, pp. 90–98.
- [2] G. A. Anderson and E. D. Jenson, "Computer interconnection structures: Taxonomy, characteristics and examples," ACM Comput. Surveys, vol. 7, pp. 197-213, Dec. 1975.
- [3] M. T. Liu, "Distributed loop computer networks," in Advances in Computers, Vol. 17. New York: Academic, 1978.
- [4] B. W. Arden and H. Lee, "Analysis of chordal ring network," *IEEE Trans. Comput.*, vol. C-30, pp. 291–295, Apr. 1981.

- [5] D. P. Agrawal, T. Y. Feng, and C. L. Wu, "A survey of communication processor systems," in Proc. COMPSAC, Chicago, IL, pp. 668-673, Nov. 1978.
- [6] A. M. Despain and D. A. Patterson, "X-tree: A tree structured multiprocessor computer architecture," in Proc. 5th Symp. on Comput. Arch., Apr. 1978, pp. 144-151.
- [7] H. Sullivan and T.R. Bashkow, "A large scale, homogeneous, fully distributed parallel machine I," in Proc. 4th Symp. Comput. Arch., Mar. 1977, pp. 105–117. L. D. Wittie, "Communication structures for large networks of micro-
- [8] computers," IEEE Trans. Comput., vol. C-30, pp. 264-273, Apr. 1981.
- [9] F. P. Preparata and J. Vullemin, "The cube connected cycles: A versatile network for parallel computation," Commun. Ass. Comput. Mach., vol. 24, pp. 300-309, May 1981.
- [10] D. K. Pradhan and S. M. Reddy, "A fault-tolerant communication architecture for distributed systems," IEEE Trans. Comput., vol. C-31, pp. 863-870, Sept. 1982.
- H. S. Stone, "Parallel processing with the perfect shuffle," IEEE Trans. [11] Comput., vol. C-20, 1971, pp. 153–161, Feb. 1971. [12] R. Finkel and M. H. Solomon, "The lens interconnection strategy," *IEEE*
- Trans. Comput., vol. C-30, pp. 960-965, Dec. 1981.
- [13] L. S. Haynes et al., "A survey of highly parallel computing," Computer, vol. 15, pp. 9-24, Jan. 1982.
- [14] D.H. Lawrie, "Memory-processor connection networks," Ph.D. dissertation, Univ. of Illinois, 1973.
- [15] L. N. Bhuyan and D. P. Agrawal, "Design and performance of a general class of interconnection networks," in Proc. 1982 Int. Conf. on Parallel Processing, Bellaire, MI, Aug. 1982, pp. 2-9; see also, IEEE Trans. Comput., vol. C-32, Dec. 1983.
- [16] J.G. Kuhl, "Fault-diagnosis in computing networks," Univ. of Iowa, ECE Tech. Rep. R-80-1, Aug. 1980, 183 pages.
- L. Kleinrock, Queueing Systems: Vol. II, Computer Applications. [17] New York: Wiley, 1976.
- K. Bhat, "On the properties of arbitrary hypercubes," Computer and [18] Mathematics with Applications, to be published.
- [19] T. Y. Feng, "A survey of interconnection networks," Computer, vol. 14, pp. 12-27, Dec. 1981.
- [20] H. J. Siegel and R. J. McMillan, "The multistage cube: A versatile interconnection network," Computer, pp. 458-473, Dec. 1981.
- D. P. Agrawal, "Graph theoretic analysis and design of multistage inter-[21] connection networks," IEEE Trans. Comput., vol. C-32, pp. 637-648, July 1983.
- [22] W. A. Wulf and C. G. Bell, "C.mmp-A multiminiprocessor," in Proc. AFIPS, Fall Joint Comput. Conf., Dec. 1972, pp. 765-777
- [23] R.J. McMillan, G.B. Adams, III, and H.J. Siegel, "Performance and implementation of  $4 \times 4$  switching modes in an interconnection network for PASM," in Proc. 1981 Int. Conf. on Parallel Processing, Aug. 1981, pp. 229-233.
- [24] L. N. Bhuyan and D. P. Agrawal, "VLSI performance of multistage interconnection networks using 4 \* 4 switches," in Proc. 3rd Int. Conf. on Distributed Computing Systems, Oct. 1982, pp. 606-613.



Laxmi N. Bhuyan (S'81-M'83) received the M.Sc. degree in electrical engineering from Regional Engineering College, Rourkela, Sambalpur University, India. in 1979, and the Ph.D. degree in computer engineering from Wayne State University, Detroit, MI, in 1982.

During 1982-83, he taught at the University of Manitoba, Winnipeg, Canada. Since September 1983, he has been with the Department of Electrical and Computer Engineering, University of Southwestern Louisiana, Lafayette, as an Assistant

Professor. His research interests include parallel and distributed computer architecture, VLSI layout, and multiprocessor performance evaluations. Dr. Bhuyan is a member of the Association for Computing Machinery.



Dharma P. Agrawal (M'74-SM'79) was born in Balod, M.P., India, on April 12, 1945. He received the B.E. degree in electrical engineering from the Ravishankar University, Raipur, M.P., India, in 1966, the M.E. (Hons.) degree in electronics and communication engineering from the University of Roorkee, Roorkee, U.P., India in 1968, and the D.Sc. Tech. degree from Federal Institute of Technology, Lausanne, Switzerland in 1975.

He has been a member of the faculty in the M.N. Regional Engineering College, Alahabad, India, the

University of Roorkee, Roorkee, India, the Federal Institute of Technology, Lausanne, Switzerland, the University of Technology, Baghdad, Iraq; Southern Methodist University, Dallas, TX, and Wayne State University, Detroit, MI. Currently, he is with the North Carolina State University, Raleigh, NC, as an Associate Professor in the Department of Electrical and Computer Engineering. His research interests include parallel/distributed processing, computer architecture, computer arithmetic, fault tolerance, and information retrieval. He has served as a referee for various reputed journals and international conferences. He was a member of Program Committees for the COMPCON Fall of 1979, the Sixth IEEE Symposium on Computer Arithmetic, and Seventh Symposium on Computer Arithmetic held in Aarhus, Denmark in June 1983. Currently, he is a member and the Secretary of the Publications Board, IEEE Computer Society, and recently, he has been appointed as the Chairman of the Rules of Practice Committee of the PUBS Board. He served as the Treasurer of the IEEE-CS Technical Committee on Computer Architecture and has been named as the Program Chairman for the 13th International Symposium on Computer Architecture to be held in Ann Arbor in June, 1984. He is also a distinguished visitor of the IEEE Computer Society.

Dr. Agrawal is a member of the ACM, SIAM, and Sigma Xi. He is listed in Who's Who in the Midwest, the 1981 Outstanding Young Men of America, and in the Directory of World Researchers' 1980's subjects published by the International Technical Information Institute, Tokyo, Japan.